DESCRIPTION

Demonstration circuit 757-A/-B features the LTC4302-1/LTC4302-2, an Addressable 2-Wire I²C bus and SMBus compatible Bus Buffer. The LTC4302-1/LTC4302-2 allows a peripheral board to be inserted and removed from a live backplane without corruption of the bus. The LTC4302-1/LTC4302-2 maintain electrical isolation between the backplane and peripheral board until their V_{CC} supply is valid and a master device on the backplane side addresses the LTC4302-1/LTC4302-2 and commands them to connect. The LTC4302-1/LTC4302-2 ADDRESS pin provides 32 possible addresses set by an external resistive divider between V_{CC} and GND. The LTC4302-1/LTC4302-2 work with supply voltages ranging from 2.7V to 5.5V. The SDA and SCL inputs and outputs do not load the bus lines when V_{CC} is low.

Rise time accelerator circuitry allows for heavier capacitive bus loading while still meeting system timing requirements. During insertion, the SDA and SCL lines are precharged to 1V to minimize bus disturbances. Two general purpose input/output pins (GPIOs) on the LTC4302-1 can be configured as inputs, open-drain outputs or push-pull outputs. The status of a GPIO is displayed with an LED on the DC757-A/-B. The LTC4302-2 option replaces one GPIO pin with a second supply voltage pin V_{CC2}, providing level shifting between systems with different supply voltages.

The DC757-A/-B is a part of the QuickEval systems which allows for quick and easy evaluation of the LTC4302-1/LTC4302-2 with a software interface.

Design files for this circuit board are available. Call the LTC factory.

OPERATION

For operation with the DC757-A/-B, connect the backplane side supply of 2.7V to 5.5V to Vcc (as shown in Figure 1). For the DC757-B, with the LTC4302-2, connect the card side supply (2.7V to 5.5V) to V_{CC2}. The backplane SDA and SCL are connected to SDAIN and SCLIN respectively while the card side bus lines are connected to SDAOUT and SCLOUT. The host controller on the backplane side first addresses and configures the LTC4302-1/LTC4302-2 to connect the backplane to card side. Communication between the backplane and card side components are then established and a host controller on either side can then control the LTC4302-1/LTC4302-2. Additional configurations include enabling and disabling the rise time accelerators on the backplane side and/or the card side, setting the GPIO(s) to open-drain output, push-pull output, or input mode, and setting or resetting the GPIO(s) outputs. A host controller can also read the internal registers of the LTC4302-1/LTC4302-2.

The CONN pin, when pulled low, resets the LTC4302-1/LTC4302-2 to its registers default state and disables communication to it. Communication can be reestablished when CONN is released high.

On the DC757-A/-B, the board's default values for resistors R1 and R2 are 1.87kΩ and 2kΩ respectively and set the address of the LTC4302-1/LTC4302-2 to $(111\ 0000)_2$. For different addressing on multiple LTC4302-1/LTC4302-2s daisy chained on the same back plane, the resistors can be changed to values suggested in Table 1 of the data sheet.

The DC757 can be configured for either a –A or –B. For a –A board, U1 is an LTC4302-1, R13A pulls up the output lines and GPIOs to Vcc, and R13B and C2 are re-

moved. To change to a –B board, use an LTC4302-2 for U1, remove R13A, R9 and D2, and add C2 and R13B to connect the Vcc2 pin to the corresponding test turret.

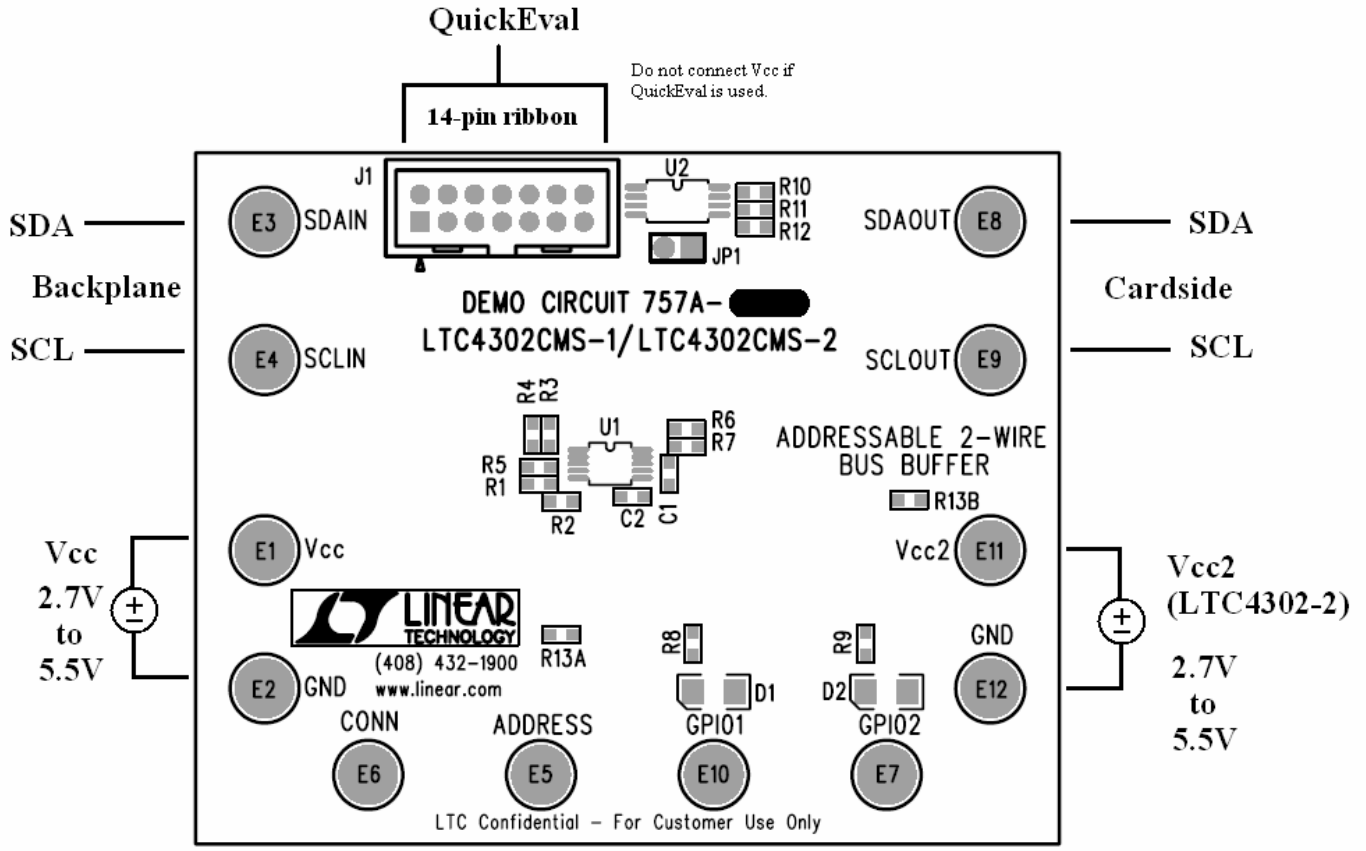


Figure 1. DC757-A/-B Equipment Setup

QUICKEVAL SETUP

The DC757-A/-B connects to the QuickEval USB Controller DC590A via 14-pin ribbon cable. The DC590A is connected to a USB port on a PC. When the QuickEval software is opened, QuickEval will detect the DC757-A/-B and bring up the LTC4302-1/LTC4302-2 software interface (shown in Figure 2). Vcc is supplied from the DC590A and an external supply is not needed. V_{CC2} however will still require power on the DC757-B.

Operation with the software interface starts with the selection of an address. Listed in the drop down menu are the 32 possible addresses for the LTC4302-1/LTC4302-2. By clicking the Find Address button, the software scans through the addresses and lists which addresses respond with an Acknowledge. Select the address for the LTC4302-1/LTC4302-2 to be communicated with.

The LTC4302-1/LTC4302-2 has two Read/Write internal registers. Checking a bit on the interface sets the corresponding bit to a 1 and unchecking sets it to 0. The first data byte is read when Read First is clicked or a bit in the first register is changed. A two data byte read is carried out when Read Both is clicked or a bit in the second register is changed. The status display for each bit is updated after a read.

The Live Running Bus check box enables a timer that sends a bogus $(0101\ 0101)_2$ data byte on the backplane bus lines every 100ms. This can be used for evaluation of the LTC4302-1/LTC4302-2 features. Connect a scope

probe on SCLIN and on SCLOUT then check the Live Running Bus. Check and uncheck the Connect bit to view on the scope the connection of the backplane to the card side and then the electrical isolation between the two. Enable and disable the rise time accelerators to view the difference in rise times.

Note: The DC590A board has its own bi-directional buffering that may have an affect with the rise time accelerators of the LTC4302-1/LTC4302-2. Viewing the data lines with the data sent from the DC590A is not a true and accurate observation of the performance of the LTC4302-1/LTC4302-2. It is best to look at the clock lines when using the DC590A.

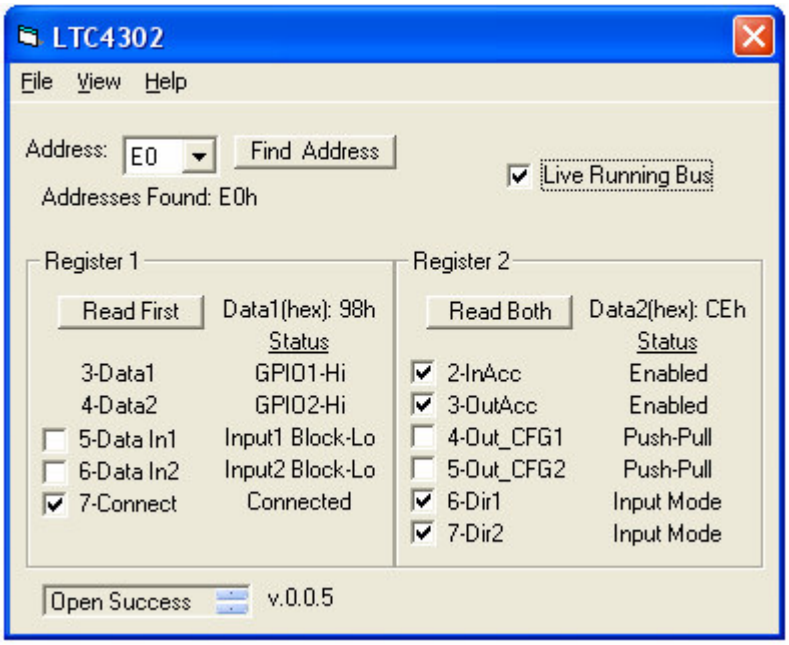
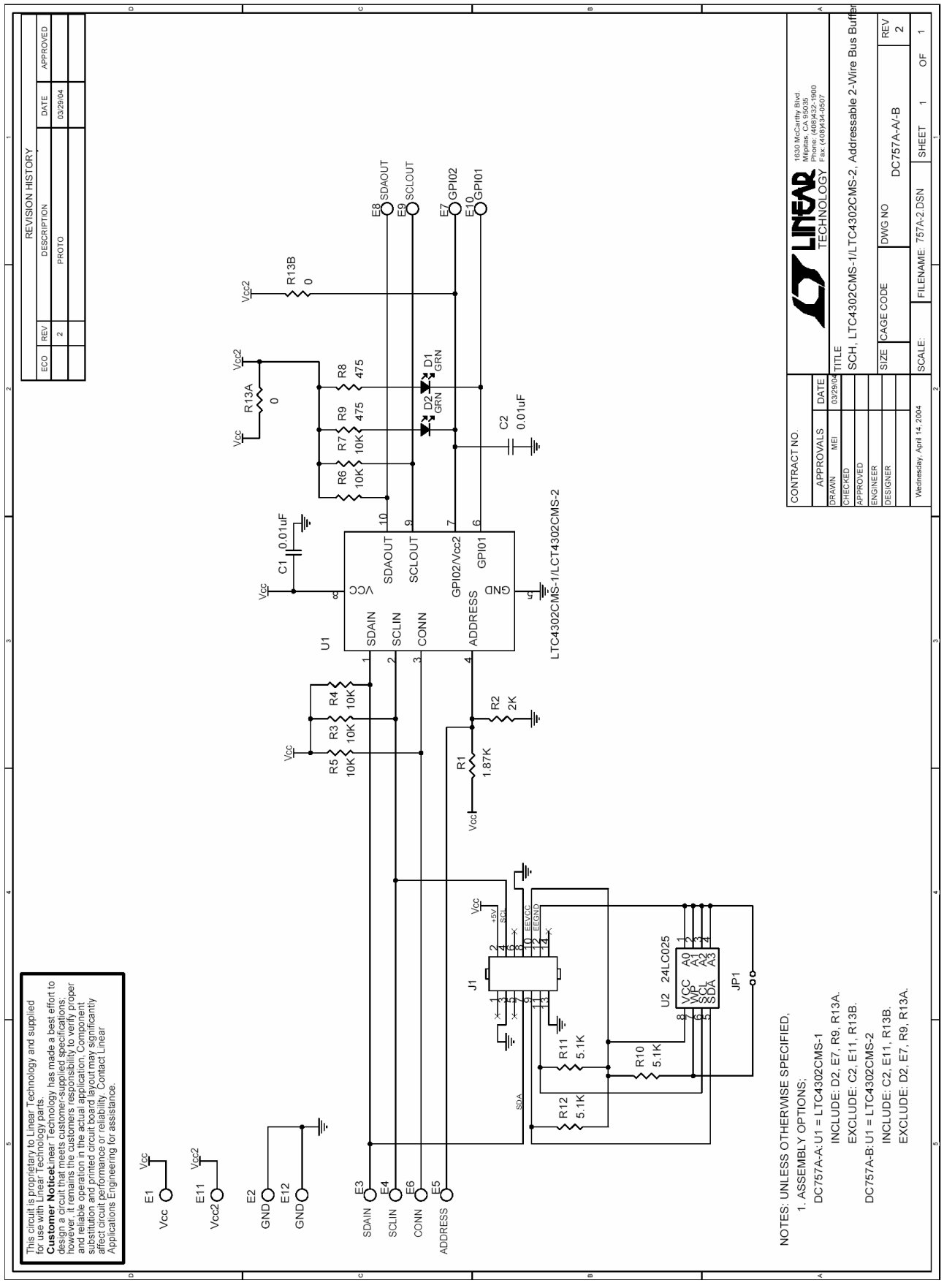


Figure 2. LTC4302-1/LTC4302-2 QuickEval Interface


REVISION HISTORY
ECO
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DESCRIPTION
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APPROVED
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03/29/04
This circuit is proprietary to Linear Technology and supplied for use with Linear Technology parts.
Customer Notice: Linear Technology has made a best effort to design a circuit that meets customer-supplied specifications; however, it remains the customers responsibility to verify proper and reliable operation in the actual application. Component substitution and printed circuit board layout may significantly affect circuit performance or reliability. Contact Linear Applications Engineering for assistance.
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CONTRACT NO.
APPROVALS
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DRAWN MEI 03/29/04
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DESIGNER
TITLE
SCH, LTC4302CMS-1/LTC4302CMS-2, Addressable 2-Wire Bus Buffer
SIZE
CAGE CODE
DWG NO
DC757A-A/-B
REV 2
Wednesday, April 14, 2004
SCALE:
FILENAME: 757A-2.DSN
SHEET 1 OF 1
U1
LTC4302CMS-1/LCT4302CMS-2
SDAIN
SCLIN
CONN
ADDRESS
SDAOUT
SCLOUT
GPIO2/Vcc2
GPIO1
VCC
GND
C1 0.01uF
C2 0.01uF
R1 1.87K
R2 2K
R3 10K
R4 10K
R5 10K
R6 10K
R7 10K
R8 475
R9 475
R10 5.1K
R11 5.1K
R12 5.1K
R13A 0
R13B 0
D1 GRN
D2 GRN
J1
U2 24LC025
JP1
Vcc
Vcc2
GND
E1 Vcc
E11 Vcc2
E2 GND
E12 GND
E3 SDAIN
E4 SCLIN
E6 CONN
E5 ADDRESS
E8 SDAOUT
E9 SCLOUT
E7 GPIO2
E10 GPIO1
NOTES: UNLESS OTHERWISE SPECIFIED,
1. ASSEMBLY OPTIONS;
DC757A-A: U1 = LTC4302CMS-1
INCLUDE: D2, E7, R9, R13A.
EXCLUDE: C2, E11, R13B.
DC757A-B: U1 = LTC4302CMS-2
INCLUDE: C2, E11, R13B.
EXCLUDE: D2, E7, R9, R13A.