



# STP150NF04

N-channel 40 V, 0.005  $\Omega$  typ., 80 A STripFET™II Power MOSFET  
in a TO-220 package

Datasheet — production data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STP150NF04	40 V	< 0.007 $\Omega$	80 A

- 100% avalanche tested
- Standard level gate drive

## Applications

- Switching applications

## Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

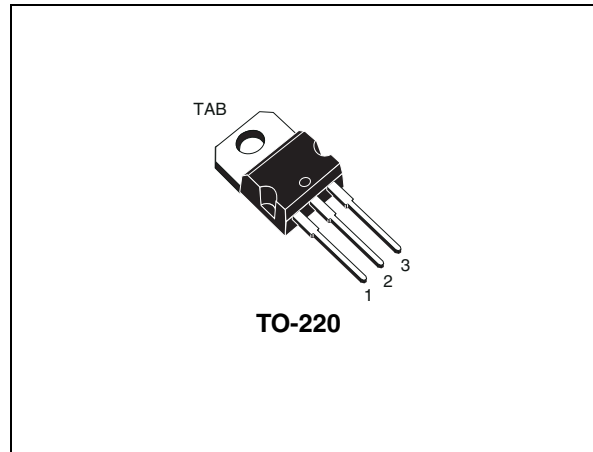


Figure 1. Internal schematic diagram

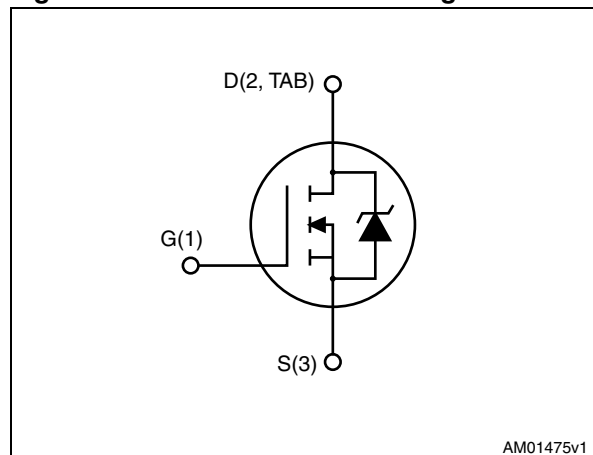


Table 1. Device summary

Order code	Marking	Package	Packaging
STP150NF04	P150NF04	TO-220	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	40	V
$V_{GS}$	Gate- source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	80	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
$P_{tot}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	2	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	0.6	J
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Max. operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 80\text{ A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\%V_{(BR)DSS}$
4. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 40\text{ A}$ ,  $V_{DD} = 30\text{ V}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	$^\circ\text{C}/\text{W}$

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz of Cu

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0$	40			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 40 \text{ V}$ $V_{DS} = 40 \text{ V} @ T_j = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 40 \text{ A}$		0.005	0.007	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15 \text{ V}$ , $I_D = 15 \text{ A}$	-	90	-	S
$C_{iss}$	Input capacitance	$V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ $V_{GS} = 0$	-	3650	-	pF
$C_{oss}$	Output capacitance			1145		pF
$C_{rss}$	Reverse transfer capacitance			400		pF
$Q_g$	Total gate charge	$V_{DD} = 32 \text{ V}$ , $I_D = 80 \text{ A}$ , $V_{GS} = 10 \text{ V}$ (see Figure 14)	-	118	150	nC
$Q_{gs}$	Gate-source charge			20	nC	
$Q_{gd}$	Gate-drain charge			45	nC	

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 25 \text{ V}$ , $I_D = 40 \text{ A}$ $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see Figure 13)	-	15	-	ns
$t_r$	Rise time			150		ns
$t_{d(off)}$	Turn-off delay time			70		ns
$t_f$	Fall time			45		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)	$I_{SD} = 80 \text{ A}, V_{GS} = 0$	-		320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80 \text{ A}, V_{GS} = 0$	-		1.3	ns nC A
$t_{rr}$	Reverse recovery time	$I_{SD} = 80 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 25 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ <i>(see Figure 15)</i>	-	73		ns
$Q_{rr}$	Reverse recovery charge			170		nC
$I_{RRM}$	Reverse recovery current			4.6		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

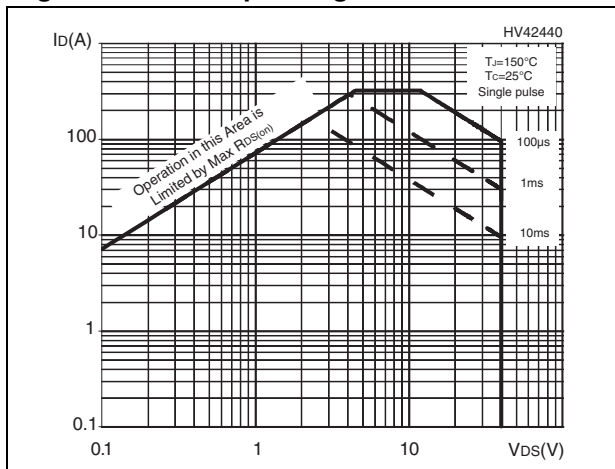


Figure 3. Thermal impedance

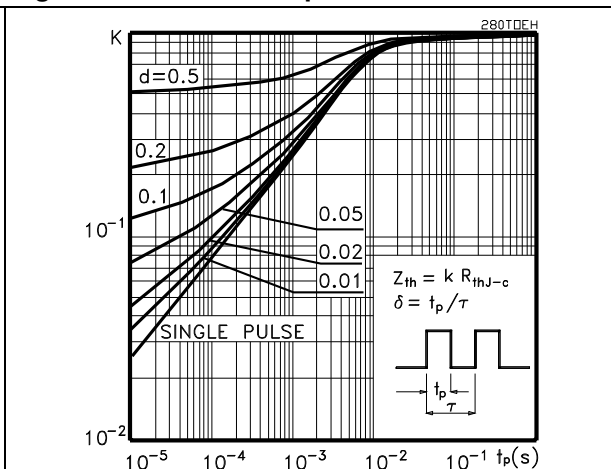


Figure 4. Output characteristics

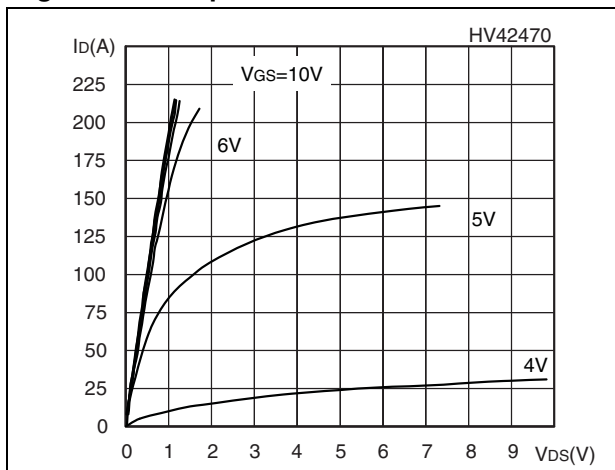


Figure 5. Transfer characteristics

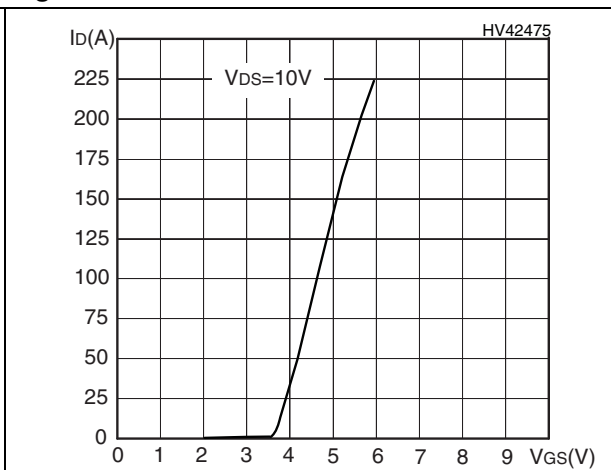


Figure 6. Normalized  $BV_{DSS}$  vs temperature

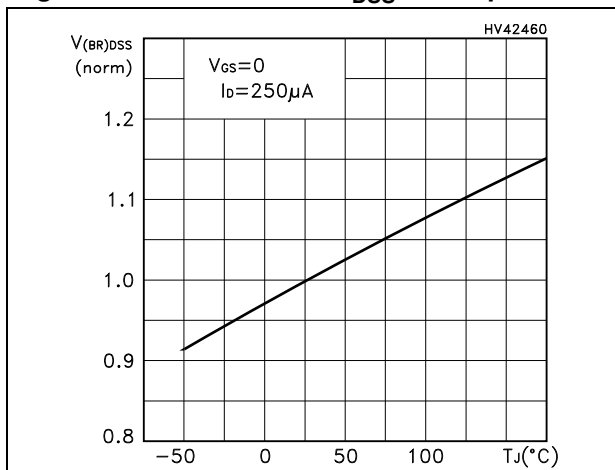


Figure 7. Static drain-source on-resistance

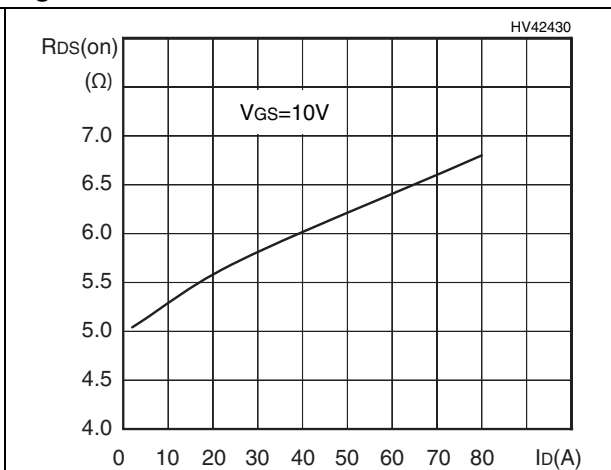


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

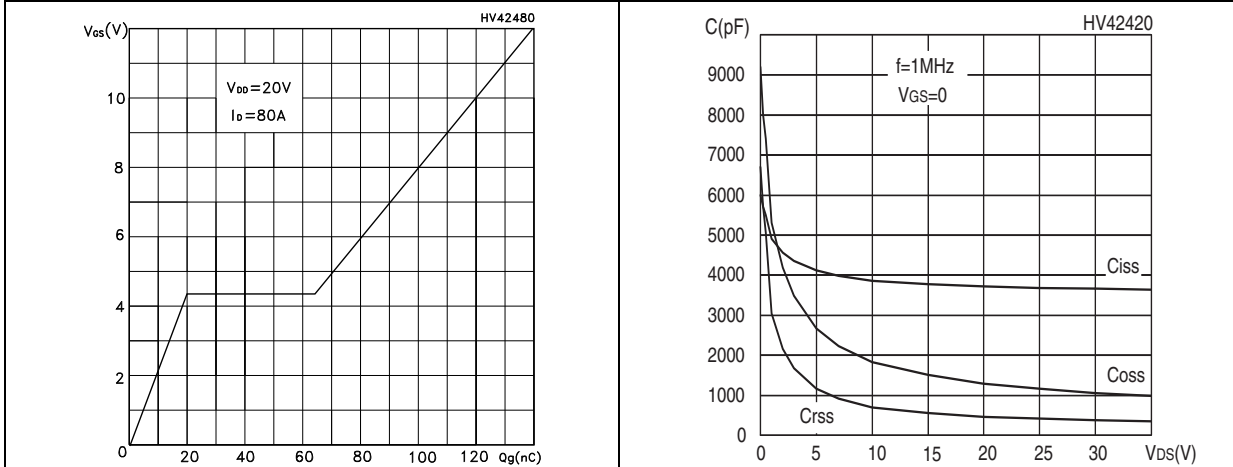


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

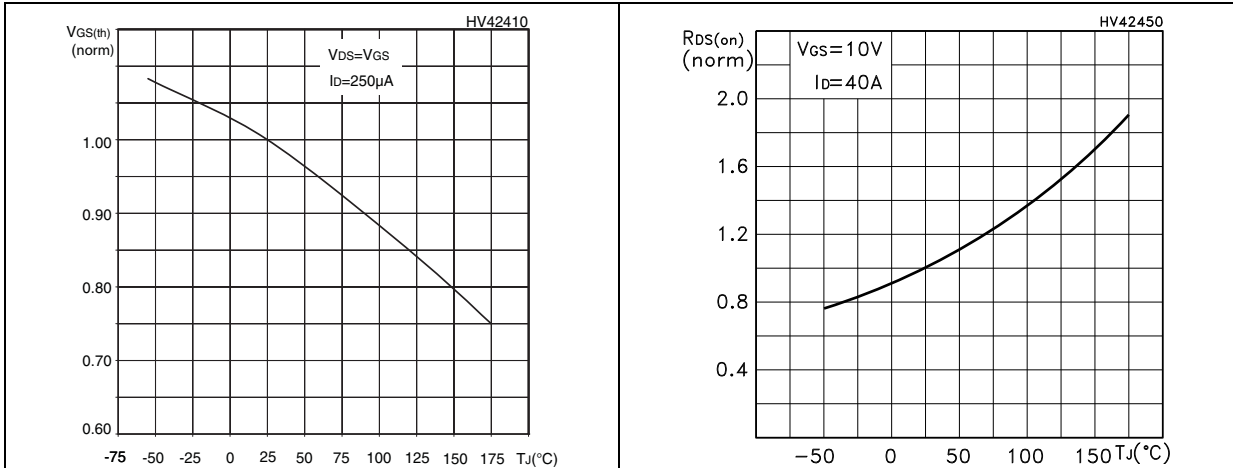
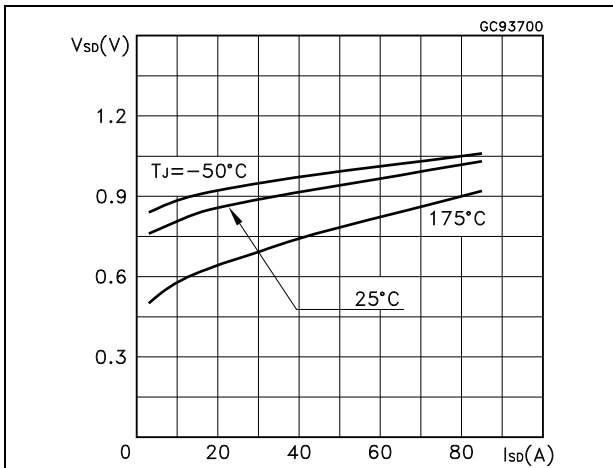
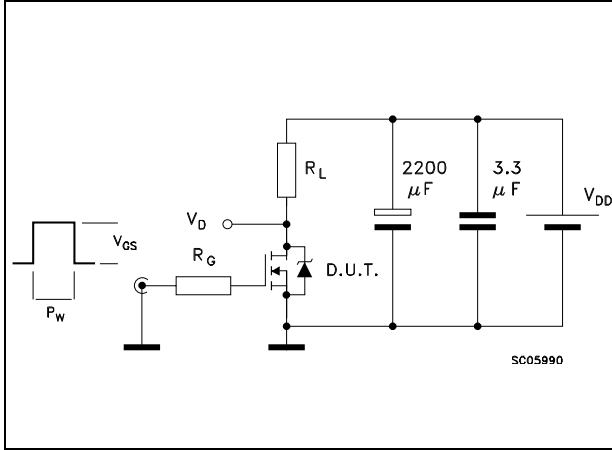


Figure 12. Source-drain diode forward characteristics

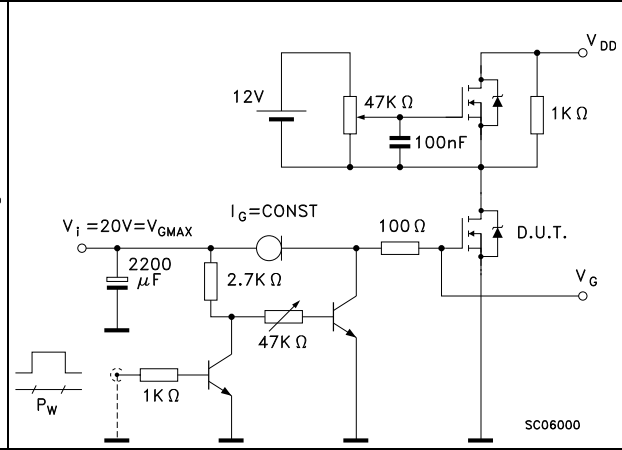


### 3 Test circuits

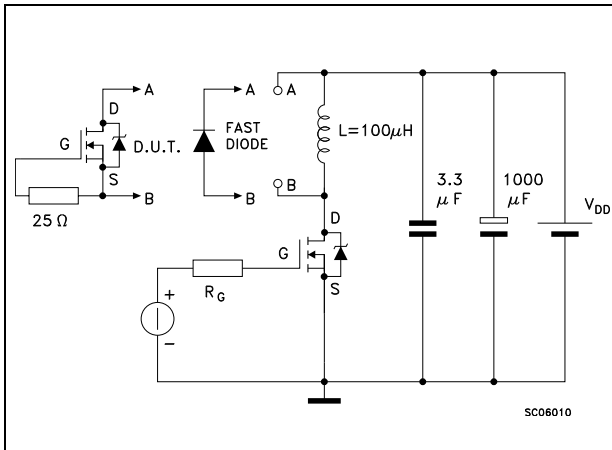
**Figure 13. Switching times test circuit for resistive load**



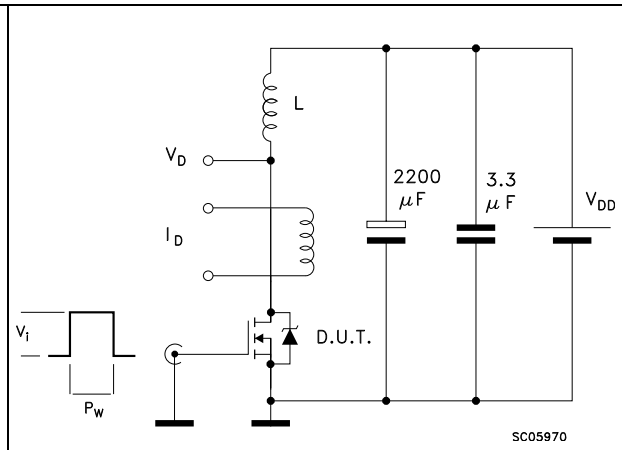
**Figure 14. Gate charge test circuit**



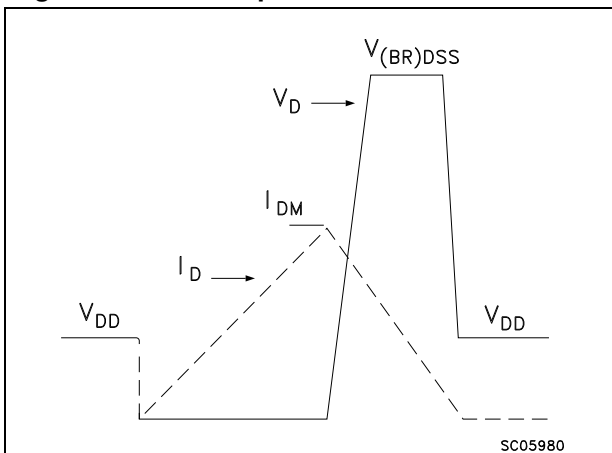
**Figure 15. Test circuit for inductive load switching and diode recovery times**



**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**





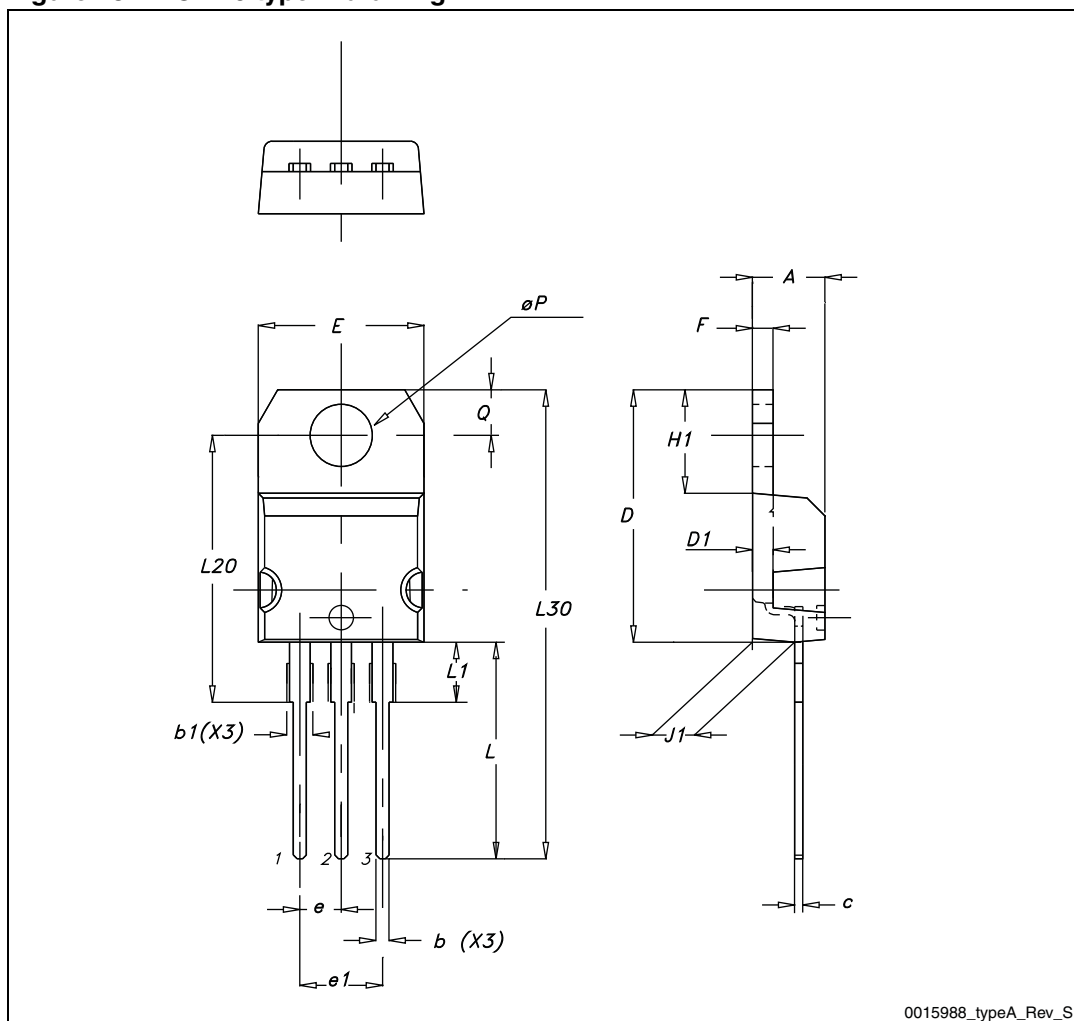
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 8. TO-220 type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 18. TO-220 type A drawing



0015988\_typeA\_Rev\_S

## 5 Revision history

**Table 9. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
01-Jul-2008	1	First release
25-Sep-2009	2	Inserted device in TO-220.
04-Oct-2012	3	Updated title and description on the cover page. Updated mechanical data.

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